Department Of Computer Application (BCA)
Dr. Rakesh Ranjan

BCA Sem - 2
Computer Organization and Architecture

Direct Memory Access logic for I/O organization

Direct memory address system were developed to address the problem of I/O mapped and interrupt driven I/O problems. In a DMA system, I/O devices can directly access the memory without intervention of the processor. DMA involves an additional module on the system bus that is capable of transfer the data to and from I/O and memory using system bus without intervention of processor. When a processor wishes to read or write a block of data , it issues a command to the DMA module. A DMA control and logic which is internal in certain processor and external in others.

Followings are sequence of operations :-

Sequence 1 –

A DMQ(DMA request) signal from an I/O device start the DMA sequence, I/O device signal an interrupt through DMA Controller(DMAC) under attention for processor.

Sequence 2-

the processor responds by checking the device's status via memory mapped control register and issue a command telling the device to do a DMA transfer.

Sequence 3-

During each successive byte transfer , the DMAC uses the processor's bus hold request line . the processor send to device from HLDA signal . the I/O bus access the address and

transfer buses of memory bus only when HLDA activate of deactivate.

Sequence 4-

which DMA transfer is complete, I/O device signals another interrupt to know to processor that DMA Done.

The sequence of event and internal DMA logic organization may be shown as :-

T; v

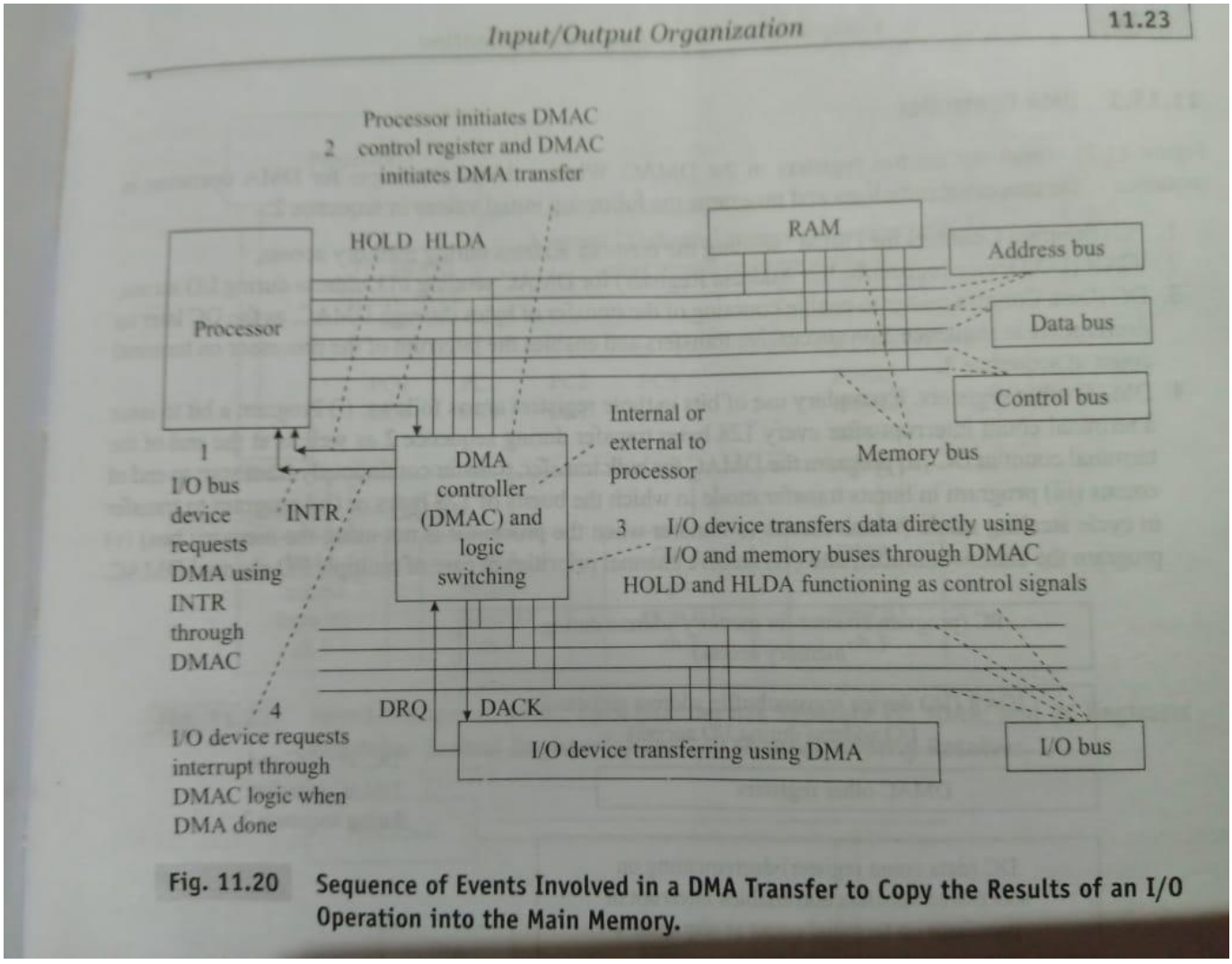


Fig. 11.20 **Sequence of Events Involved in a DMA Transfer to Copy the Results of an I/O Operation into the Main Memory.**

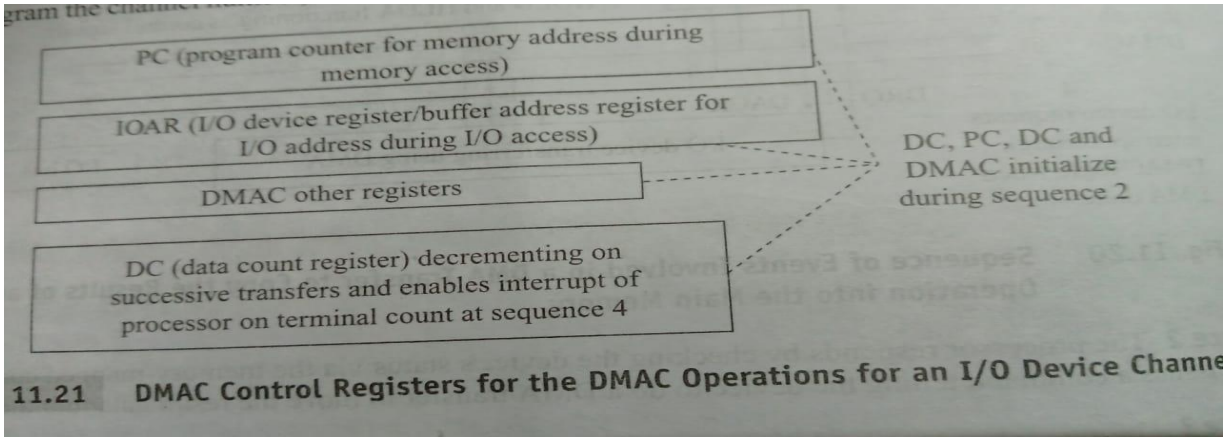
DMA Controller :-

It is generally known as DMAC. When the divice interrupts for DMA operations in sequence 1 , the processor initializes the following initial value and programs the following value in sequence 2

1. PC(program counter) for DMAC sending the memory address during memory access
2. IQAR (I/O Device buffer address register) for DMAC sending I/O address during I/O Access.
3. DC(Data count) register to enable counting of the transfer of byte through (DMAC)
4. DMAC other register use bits in these registers are as follows
    a. Program a bit to issue a terminal count interrupt after every 128 byte transfer at the end of DC count
    b. Program the DMAC for bulk transfer
    c. Program in brust transfer mode in which the brust the 128 byte
    d. Program to transfer in cycle stealing mode.

DMA I/O Channel :-

A DMAC can be multichannel because , it is used by several devices and each device may have separate PC,IQAR, and DC. Each channel have separate DMA request, DRQ,DMA ACK . One I/O channel may be allocated a for DRAM refress controller.



11.21 DMAC Control Registers for the DMAC Operations for an I/O Device Channe

----------X----------